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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,401	08/27/2003	Seok-Woo Lee	053785-5148	5327

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EXAMINER	
ISAAC, STANETTA D	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 01/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/648,401	LEE, SEOK-WOO	
	Examiner	Art Unit	
	Stanetta D. Isaac	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *26* is/are allowed.

6)☒ Claim(s) *1-7,9-22,24 and 25* is/are rejected.

7)☒ Claim(s) *8 and 23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the amendment filed on 10/28/04. Currently, claims 1-26 are pending.

Specification

The objection to the specification, in the Office Action mailed 8/03/04, has been withdrawn. The amendment to the word "first" was sufficient to correct the informalities.

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

The objection to claims, in the Office Action mailed 8/03/04, has been withdrawn. The amendment to claims 5 and 15 to change the limitation to "PECVD" was sufficient to correct the informalities.

Claim 22 is objected to because of the following informalities: In line 2, "includes" should be " including". Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-7, 9-22, 24 and 25 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamazaki et al. US Patent 6,168,980.

Yamazaki discloses the semiconductor method as claimed. See figures 1A-7E, and corresponding text, pertaining to claims 1 and 11, where Yamazaki teaches a method for forming a polysilicon thin film transistor, comprising: forming a buffer layer **102** over a substrate **101**; depositing an amorphous silicon layer **103** over a substrate; crystallizing the amorphous silicon layer into a polycrystalline silicon layer **103**; (col. 7, lines 33-59; ***Note***: that the formation of polycrystalline silicon layer is considered inherent since an amorphous silicon layer exhibits a polycrystalline structure when subjected to elevated temperatures after deposition. See *Stanley Wolf and Richard N. Tauber Vol. I, Second Edition, Silicon Processing for The VLSI ERA*, page 181, under *Properties of Polysilicon Thin Films*); patterning the polycrystalline silicon layer to form a polysilicon active layer **104, 105** for a thin film transistor; depositing silicon oxide over the polysilicon active layer to form a gate insulation layer **106** under a vacuum condition (col. 7, lines 60-67; col. 8, lines 1-10; ***Note***: that the deposition of silicon oxide being performed under a vacuum condition is considered to be inherent since Yamazaki teaches, controlling the pressure range from 0.05 to .5 Torr to deposit the silicon oxide in a PECVD or LPCVD process. In an LPCVD or PECVD process the claimed pressure range is considered to be a medium vacuum. See *Stanley Wolf and Richard N. Tauber Vol. I, Silicon Processing for The VLSI ERA*, page 169, under *Low-Pressure Chemical Vapor Deposition Reactors*); applying heat to anneal the gate insulation layer under the vacuum condition (col. 7, lines 62-67 and col. 8, lines 1-20); and forming a gate electrode **107, 108** on the annealed gate insulation layer; applying dopants to the

polysilicon active layer to form source and drain regions **109-112**; (col. 8, lines 65-68; col. 9 lines 10-34) forming an interlayer insulator **113** to cover the electrode, the gate insulation layer and the source and drain regions; forming source and drain contact holes in the interlayer insulator to expose portions of the source region and the drain region, respectively; (col. 9, lines 35-44) and forming source drain electrodes **114-116**.

Pertaining to claims 2 and 12, Yamazaki teaches the method, wherein there is no vacuum break between depositing silicon oxide to form gate insulation layer and applying heat to anneal the gate insulation layer. (col. 7, lines 62-67 and col. 8, lines 1-20; col. 12, lines 5-18; ***Note***: since there may be no evacuation of the chamber between the steps, there is no vacuum break between the steps.)

Pertaining to claims 3 and 13, Yamazaki teaches the method, wherein applying the heat to annealing the gate insulation layer is performed at a temperature ranging from 400 to 600 degrees Celsius. (col. 8, lines 10-64)

Pertaining to claims 4 and 14, Yamazaki teaches the method, wherein the vacuum condition for applying the heat to annealing the gate insulation layer is a pressure ranging from 50 to 5000 mTorr. (col. 7, lines 62-67 and col. 8, lines 1-36)

Pertaining to claims 5 and 15, Yamazaki teaches the method, wherein depositing the silicon oxide includes using a plasma enhanced chemical vapor deposition (PECVD) method. (col. 7, lines 62-67; ***Note***: it is inherent that RF plasma CVD is another terminology for PECVD. See *Stanley Wolf and Richard N. Tauber Vol. I, Silicon Processing for The VLSI ERA*, pages 171-172, under *Plasma Enhanced CVD: Physics, Chemistry, & Reactor Designs*)

Pertaining to claims 6 and 16, Yamazaki teaches the method, wherein crystallizing the amorphous silicon layer includes applying heat to the amorphous silicon layer using an excimer laser. (col. 7, lines 32-36)

Pertaining to claims 7 and 22, Yamazaki teaches the method, wherein applying heat occurs in the atmosphere of a vacuum chamber including at one of N_2, H_2, O_2, N_2O, and NO. (col. 8, lines 1-35)

Pertaining to claims 9 and 24, Yamazaki teaches the method, wherein the temperature of annealing the gate insulation layer is higher than the temperature of depositing the silicon oxide. (col. 7, line 66, col. 8, lines 10-64)

Pertaining to claims 10 and 25, Yamazaki teaches the method, wherein there is vacuum break between depositing the silicon oxide to form the gate insulation layer and applying the heat to anneal the gate insulation layer. (col. 12, lines 5-18; ***Note***: since the chamber may be evacuated to a high vacuum, there is a vacuum break between the steps.)

Pertaining to claim 17, Yamazaki teaches the method, where the buffer layer includes at least one of silicon oxide (SiO_x) and silicon nitride (SiN_x). (col. 7, lines 23-26)

Pertaining to claims 18 and 19, Yamazaki teaches the method, wherein applying dopants includes applying p-type ions that are boron ions. (col. 9, line 32)

Pertaining to claims 20 and 21, Yamazaki teaches the method, wherein applying dopants includes applying n-type ions that are phosphorous ions. (col. 9, line 31)

Allowable Subject Matter

Claims 8 and 23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Applicant's dependent claims 8 and 23, and independent claim 26, indicate allowable subject matter over the prior art of record, since, the prior art fails to teach or render obvious the method "wherein, the difference of flat band voltage (Δ Vfb) between initial flat band voltage [Vfb(initial)] and flat band voltage after Fowler-Nordheim stress [Vfb(FNS)] is less than 0.5V after applying the heat to anneal the gate insulation layer."

Response to Arguments

Applicant's arguments filed on 10/28/04 have been fully considered but they are not persuasive.

In response to applicant's Remarks, pages 11-13:

Applicant raises the clear issue of whether Yamazaki teaches or suggests the claimed combination including at least the feature of "depositing silicon oxide over the polysilicon active layer to form a gate insulation layer under a vacuum condition" and "applying heat to anneal the gate insulation layer under the vacuum condition."

The Examiner takes the position that the method of forming a polysilicon thin film transistor, as shown in Yamazaki, (figures 1A-7E), ~~and~~ teaches "depositing silicon oxide over the

polysilicon active layer to form a gate insulation layer under a vacuum condition" and "applying heat to anneal the gate insulation layer under the vacuum condition." (col. 7, lines 62-67; col. 8, lines 1-20)

In response to the Applicant's Remarks, pages 11-13, Applicant does not claim the deposition step in the same chamber, making the argument a moot point. However, assuming ~~arguments~~ that the limitation was included in the claims, the Examiner disagrees that Yamazaki does not teach or suggest "depositing the silicon oxide film under the vacuum condition in the same chamber 301." The Examiner has reviewed the prior art of record in its entirety, and has not found any evidence or suggestion of the use of an additional vacuum chamber. Specifically, as stated for example in col. 7, lines 62-67 and col. 8, lines 1-20, Yamazaki teaches that the silicon oxide film is formed by "RF plasma CVD while controlling the temperature of the substrate in the range of from 200 to 500°C..." and that "The resulting silicon oxide film was thermally annealed at 400 to 700°C in an atmosphere comprising a nitrogen gas." In these steps there is no implicit statement or suggestion that an additional chamber is being used to perform this step between depositing the silicon oxide film and annealing the silicon oxide film. Furthermore, as stated in col. 11, lines 51-67 and col. 12, lines 1-18, the silicon oxide film is formed by RF plasma CVD and annealed by a laser beam and an intense light. Once again there is no statement suggesting that an additional chamber has been included between these processing steps. With regard to the vacuum conditions, as stated in col. 8, lines 1-11, the pressure ratio as well as the pressure ranges are disclosed within the teachings of Yamazaki during these processing steps, where the only changing variable within these steps is with regards to the temperature. Therefore, since the only changing variable within these processing

steps is the temperature, then vacuum conditions must implicitly be the same under both steps of depositing and annealing the silicon oxide film.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stanetta Isaac
Patent Examiner
January 14, 2005

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